Program: BE Electronics and Telecommunication Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester VI

Course Code: ECCDLO6021 Course Name: Digital VLSI Design

Time: 1 hour Max. Marks: 50

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Note to the students: - All the Questions are compulsory and carry equal marks.

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| Q1. | In VLSI design, which process deals with the determination of resistance & capacitance of interconnections? |
| Option A: | Floorplanning |
| Option B: | Placement & Routing |
| Option C: | Testing |
| Option D: | Extraction |
|  |  |
| Q2. | Pass transistor can be driven through \_\_\_\_\_ pass transistors |
| Option A: | One |
| Option B: | More |
| Option C: | No |
| Option D: | Two |
|  |  |
| Q3. | Main electronic device of VLSI technology is |
| Option A: | Diode |
| Option B: | Digital Signal |
| Option C: | Junction Field Effect Transistor (JFET) |
| Option D: | Transistor |
|  |  |
| Q4. | In static CMOS circuit, number of PMOS are ------------as compare to number of NMOS |
| Option A: | Less than |
| Option B: | More than |
| Option C: | Equal |
| Option D: | Not predicted |
|  |  |
| Q5. | In pseudo NMOS circuit GATE of PMOS is connected to ------ |
| Option A: | DRAIN of NMOS |
| Option B: | GATE of NMOS |
| Option C: | Ground |
| Option D: | Source of PMOS |
|  |  |
|  |  |
| Q6. | Precharge & evaluate logic is in |
| Option A: | Dynamic logic |
| Option B: | Pass transistor |
| Option C: | CPL |
| Option D: | Transmission gate |
|  |  |
| Q7. | CCMOS is also called as |
| Option A: | Clocked CMOS |
| Option B: | Complementory CMOS |
| Option C: | Charge CMOS |
| Option D: | Coupled CMOS |
|  |  |
| Q8. | Why is SRAM more preferably in volatile memory? |
| Option A: | low-cost |
| Option B: | high-cost |
| Option C: | Fast |
| Option D: | transistor as a storage element |
|  |  |
| Q9. | --------- Number of PMOS transistors are required to design 2 input NAND gate using CMOS technique. |
| Option A: | 1 |
| Option B: | 2 |
| Option C: | 3 |
| Option D: | 4 |
|  |  |
| Q10. | Which type of storage element of SRAM is very fast in accessing data but consumes lots of power? |
| Option A: | CMOS |
| Option B: | TTL |
| Option C: | NAND |
| Option D: | NOR |
|  |  |
| Q11. | Fast-look-ahead carry circuits found in most 4-bit full-adder circuits which ------------ |
| Option A: | Increase ripple delay |
| Option B: | Add a 1 to complemented inputs |
| Option C: | Reduce propagation delay |
| Option D: | Determine sign and magnitude |
|  |  |
| Q12. | What distinguishes the look-ahead-carry adder? |
| Option A: | It is faster than a ripple-carry adder |
| Option B: | It is slower than the ripple-carry adder |
| Option C: | It is easier to implement logically than a full adder |
| Option D: | It requires advance knowledge of the final answer |
|  |  |
| Q13. | What is one disadvantage of the ripple-carry adder? |
| Option A: | More stages are required to a full adder |
| Option B: | It is slow due to propagation time |
| Option C: | The interconnections are more complex |
| Option D: | More stages are required to a full and Half adder |
|  |  |
| Q14. | The component used in DRAM is |
| Option A: | Capacitor |
| Option B: | Inductor |
| Option C: | JFET |
| Option D: | Resistor |
|  |  |
| Q15. | When capacitor voltage is zero ,DRAM will store |
| Option A: | 0 |
| Option B: | 1 |
| Option C: | 0 and 1 |
| Option D: | Retain previous value |
|  |  |
| Q16. | Clocked sequential circuits are |
| Option A: | four phase non overlapping clock |
| Option B: | four phase overlapping clock |
| Option C: | two phase non overlapping clock |
| Option D: | two phase overlapping clock |
|  |  |
| Q17. | ---------- is used to drive high capacitance load. |
| Option A: | single polar capability |
| Option B: | bipolar capability |
| Option C: | tripolar capability |
| Option D: | nullpolar capability |
|  |  |
| Q18. | Non inverting dynamic register storage cell consists of -------- transistors for nMOS and --------- for CMOS. |
| Option A: | six, eight |
| Option B: | eight, six |
| Option C: | five, six |
| Option D: | six, five |
|  |  |
| Q19. | What is the inputs in the PLD is given through\_\_\_\_\_ |
| Option A: | OR gates |
| Option B: | NAND gates |
| Option C: | AND gates |
| Option D: | NOR gates |
|  |  |
| Q20. | What are the Outputs of AND gate in PLD is said to be \_\_ |
| Option A: | Both input and output same |
| Option B: | Output lines |
| Option C: | Strobe lines |
| Option D: | Input lines |
|  |  |
| Q21. | Which type of PLD should be used, for programmable logic functions? |
| Option A: | PAL |
| Option B: | SLD |
| Option C: | PLA |
| Option D: | CPLD |
|  |  |
| Q22. | In VHDL instructions are executed in ---------- way. |
| Option A: | Concurrent |
| Option B: | Sequential |
| Option C: | Net-list |
| Option D: | Test Bench |
|  |  |
| Q23. | RTL is a design abstraction of what kind of circuit? |
| Option A: | Asynchronous digital circuit |
| Option B: | Asynchronous sequential circuit |
| Option C: | Synchronous digital circuit |
| Option D: | Analog circuit |
|  |  |
| Q24. | RTL is used in HDL to create what level of representations in the circuit? |
| Option A: | Low-level |
| Option B: | High-level |
| Option C: | Mid-level |
| Option D: | Same level |
|  |  |
| Q25. | Which flip-flop is usually used in the implementation of the registers? |
| Option A: | D-FF |
| Option B: | T-FF |
| Option C: | JK-FF |
| Option D: | SR-latch |