Program: BE Electronics Engineering

Curriculum Scheme: Revised 2012

Examination: Final Year Semester VIII

Course Code: EXC801 and Course Name: CMOS VLSI Design

Time: 1hour Max. Marks: 50

Note to the students: - All the Questions are compulsory and carry equal marks.

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| Q1. | The important feature of current mirror circuit is: - |
| Option A: | high output resistance & high input resistance |
| Option B: | low output resistance & low input resistance |
| Option C: | low output resistance & high input resistance |
| Option D: | high output resistance & low input resistance |
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| Q2. | Body effect can be eliminated by tying \_\_\_\_\_\_\_\_\_\_\_ & \_\_\_\_\_\_\_\_\_\_\_\_ of each PMOS transistor, in simple circuit to establish supply independent currents. . |
| Option A: | drain terminal & bulk terminal |
| Option B: | source terminal & drain terminal |
| Option C: | source terminal & bulk terminal |
| Option D: | source terminal & gate terminal |
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| Q3. | For obtaining a reference voltage, select appropriate equation, with zero TC. |
| Option A: | VREF = α1V1 + α2V2 |
| Option B: | VREF = α1V1 - α2V2 |
| Option C: | VREF = α1V1 \* α2V2 |
| Option D: | VREF = α1V1/ α2V2 |
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| Q4. | Among various device parameters in semiconductor technologies, the characteristics of \_\_\_\_\_\_\_\_\_\_\_\_\_\_have proven the most reproducible and well-defined quantities that can provide positive and negative TCs. |
| Option A: | MOSFET |
| Option B: | Bipolar transistors |
| Option C: | JFET |
| Option D: | MESFET |
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| Q5. | The maximum output voltage of CS amplifier can be achieved with diode connected load is |
| Option A: | Vout,max=VDD -VTH |
| Option B: | Vout,max=VDD |
| Option C: | Vout,max=VDD+VTH |
| Option D: | Vout,max=- -VDD |
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| Q6. | The drawbacks of source follower namely |
| Option A: | non-linearity due to body effect |
| Option B: | linearity due to body effect |
| Option C: | better driving capability |
| Option D: | maximum output voltage |
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| Q7. | In which amplifier senses the input at the source and produces the output at the drain |
| Option A: | CS amplifier |
| Option B: | CG amplifier |
| Option C: | CD amplifier |
| Option D: | CS amplifier with source degeneration |
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| Q8. | The linear behavior of a CS stage using a diode-connected load can be accomplished by placing |
| Option A: | a diode in series with source terminal |
| Option B: | A degeneration resistor in series with the source terminal. |
| Option C: | A capacitor in series with source terminal |
| Option D: | Source terminal to ground without resistor |
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| Q9. | The gain of CS stage can be maximized by replacing the load resistor |
| Option A: | With diode connected load |
| Option B: | With triode load |
| Option C: | With a current source |
| Option D: | With capacitor |
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| Q10. | The useful property of differential signaling is |
| Option A: | infinite voltage gain |
| Option B: | zero voltage gain |
| Option C: | decrease in maximum achievable voltage swing |
| Option D: | increase in maximum achievable voltage swing |
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| Q11. | The Maximum and minimum output of the Differential amplifiers is defined as: |
| Option A: | Vmax = VDD, Vmin = -VDD |
| Option B: | Vmax = VDD, Vmin = Rd.Iss |
| Option C: | Vmax = VDD, Vmin = VDD – Rd.Iss |
| Option D: | Vmax = VDD, Vmin = – Rd.Iss |
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| Q12. | Flicker noise originates due to: |
| Option A: | Conduction in channel |
| Option B: | Drain to Source voltage |
| Option C: | Reduction in channel length |
| Option D: | Dangling bonds |
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| Q13. | Transconductance can be increased by \_\_\_\_\_\_\_\_\_\_\_ |
| Option A: | Decreasing the width |
| Option B: | Increasing the width |
| Option C: | Keeping width constant |
| Option D: | Decreasing width keeping W/L ratio constant |
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| Q14. | The ohmic section of a MOSFET contributes |
| Option A: | Flicker noise |
| Option B: | Thermal noise |
| Option C: | Zero noise |
| Option D: | White noise |
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| Q15. | In which of the following configuration is the input resistance (Ri) not equal to zero ideally? |
| Option A: | Common source configuration |
| Option B: | Common source configuration with source resistance |
| Option C: | Common gate configuration |
| Option D: | Source follower configuration |
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| Q16. | With respect to Root locus of Single pole system, a real valued pole in left half plane moves \_\_\_\_\_\_\_ the origin as loop gain \_\_\_\_\_\_. |
| Option A: | Towards, Increases |
| Option B: | Towards, Decreases |
| Option C: | Away from, Decreases |
| Option D: | Away from, Increases |
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| Q17. | Stability of OPAMP can be achieved by \_\_\_\_\_\_\_ the overall phase-shift and \_\_\_\_\_\_ the gain. |
| Option A: | maximizing, raising |
| Option B: | maximizing, dropping |
| Option C: | minimizing, raising |
| Option D: | minimizing, dropping |
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| Q18. | In Miller compensation of two stage OPAMP, the compensating capacitor CC is connected |
| Option A: | at the input of stage one |
| Option B: | at the output of stage two |
| Option C: | at the output of stage one |
| Option D: | between the input and output of stage two |
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| Q19. | What happens when the operating frequency of an op-amp increase? |
| Option A: | Gain of the amplifier decrease |
| Option B: | Phase shift between output and input signal decrease |
| Option C: | Gain and phase shift of amplifier decreases |
| Option D: | Gain and phase shift of amplifier increases |
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| Q20. | In Switched-capacitor amplifier circuit, what is our assumption, before we study the circuit in two phases. |
| Option A: | that the open-loop gain of the op amp is very small |
| Option B: | that the closed-loop gain of the op amp is very large |
| Option C: | that the open-loop gain of the op amp is zero. |
| Option D: | that the open-loop gain of the op amp is very large |
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| Q21. | What happens in Channel Charge Injection? |
| Option A: | When the switch turns off, Qch exits through the source and drain terminals |
| Option B: | When the switch turns on, Qch exits through the source and drain terminals |
| Option C: | When the switch turns off, Qch enters through the source and drain terminals |
| Option D: | When the switch turns on, Qch enters through the source and drain terminals |
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| Q22. | Even for clock feedthrough mechanism, the circuit does not provide complete cancellation because \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| Option A: | the gate-source overlap capacitance of NFETs is not equal to that of PFETs |
| Option B: | the gate-drain overlap capacitance of NFETs is equal to that of PFETs |
| Option C: | the gate-source overlap capacitance of NFETs is equal to that of PFETs |
| Option D: | the gate-drain overlap capacitance of NFETs is not equal to that of PFETs |
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| Q23. | In the circuit of figure, continuous-time feedback amplifier, the closed-loop gain is set by the ratio of R2 and R1, in order to avoid reducing the open-loop gain of the op amp, we postulate that the resistors can be replaced by \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_. |
| Option A: | Inductors |
| Option B: | Transistors |
| Option C: | Diodes |
| Option D: | Capacitors |
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| Q24. | Which of the following represents the charging time of capacitor to maximum input value? |
| Option A: | Time constant of circuit |
| Option B: | Acquisition time |
| Option C: | Peak time |
| Option D: | Threshold time |
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| Q25. | Which type of ADC follow the conversion technique of changing the analog input signal to a linear function of frequency? |
| Option A: | Direct type ADC |
| Option B: | Integrating type ADC |
| Option C: | Pipeline ADC |
| Option D: | Successive approximation ADC |