Program: BE Computer Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester V

Course Code: CSC501 and Course Name: Microprocessor

Time: 1 hour Max. Marks: 50

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Note to the students:- All the Questions are compulsory and carry equal marks .

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| Q1. | Which is not the control bus signal: |
| Option A: | READ |
| Option B: | WRITE |
| Option C: | RESET |
| Option D: | CLR |
|  |  |
| Q2. | By what factor does the 8284A clock generator divide the crystal oscillator’s output frequency? |
| Option A: | 1 |
| Option B: | 2 |
| Option C: | 3 |
| Option D: | 4 |
|  |  |
| Q3. | IC 8288 Bus controller is an \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ pin chip |
| Option A: | 32 |
| Option B: | 40 |
| Option C: | 18 |
| Option D: | 20 |
|  |  |
| Q4. | Which of the following statement is true? |
| Option A: | The group of machine cycle is called a state. |
| Option B: | A machine cycle consists of one or more instruction cycle. |
| Option C: | An instruction cycle is made up of machine cycles and a machine cycle is made up of number of states. |
| Option D: | None of the above |
|  |  |
| Q5. | If MN/MX (bar) is low, the 8086 operates in \_\_\_\_\_ mode. |
| Option A: | Minimum mode |
| Option B: | Maximum mode |
| Option C: | Interrupt mode |
| Option D: | Control mode |
|  |  |
| Q6. | MOV CL, [BX] is an example of which addressing mode? |
| Option A: | Immediate addressing mode |
| Option B: | Register addressing mode |
| Option C: | Direct addressing mode |
| Option D: | Indirect addressing mode |
|  |  |
| Q7. | Assume AL = 1001 0101 , BL = 0101 1011  After the following instruction what will be the value in AL and BL?  AND AL, BL |
| Option A: | AL = 1001 0101 , BL = 0001 0001 |
| Option B: | AL = 0001 0001 , BL = 0101 1011 |
| Option C: | AL = 0001 0001 , BL = 0001 0001 |
| Option D: | AL = 1001 0101 , BL = 0101 1011 |
|  |  |
| Q8. | Which of the following instruction is used to clear the carry flag? |
| Option A: | STC |
| Option B: | CLC |
| Option C: | CLR |
| Option D: | CMC |
|  |  |
| Q9. | Assume BL = 0011 0101  To clear the lower nibble of BL : |
| Option A: | AND BL with F0H |
| Option B: | OR BL with F0H |
| Option C: | AND BL with FFH |
| Option D: | Negate BL |
|  |  |
| Q10. | Assume AL= 0101 1111 ,BL=1010 1000  What is the value of ZF,CF,AF after ADD AL,BL ? |
| Option A: | ZF=0, CF=0, AF=0 |
| Option B: | ZF=1, CF=1, AF=1 |
| Option C: | ZF=1, CF=0, AF=0 |
| Option D: | ZF=0, CF=1, AF=1 |
|  |  |
| Q11. | The interrupts which can be ignored are called |
| Option A: | Polling |
| Option B: | Non Maskable |
| Option C: | Maskable |
| Option D: | Fixed |
|  |  |
| Q12. | The 8259A can be initialized with \_\_\_\_ ICWs |
| Option A: | Two |
| Option B: | Eight |
| Option C: | Four |
| Option D: | Three |
|  |  |
| Q13. | \_\_\_\_\_\_\_\_ is the process where the computer or controlling device waits for an external device to check for its readiness or state |
| Option A: | Interrupt |
| Option B: | Polling |
| Option C: | Mask |
| Option D: | Unmask |
|  |  |
| Q14. | The interrupts which are having fixed address location for ISR are called \_\_\_\_\_\_ |
| Option A: | vectored interrupt |
| Option B: | Software Interrupt |
| Option C: | non vectored interrupt |
| Option D: | Hardware Interrupt |
|  |  |
| Q15. | How many data lines in total are there in the 8255 PPI IC? |
| Option A: | 8 data lines |
| Option B: | 32 data lines |
| Option C: | 24 data lines |
| Option D: | 16 data lines |
|  |  |
| Q16. | In control word register, if SC1=0 and SC0=1, then the counter selected is |
| Option A: | counter 0 |
| Option B: | counter 1 |
| Option C: | counter 2 |
| Option D: | counter 3 |
|  |  |
| Q17. | Which of the following mode of 8255 is Strobed Bi-directional I/O? |
| Option A: | Mode 0 |
| Option B: | Mode 1 |
| Option C: | Mode 2 |
| Option D: | Mode 3 |
|  |  |
| Q18. | To address a memory location out of N memory locations, the number of address lines required is |
| Option A: | log N (to the base 2) |
| Option B: | Log N (to the base 10) |
| Option C: | log N (to the base e) |
| Option D: | log (2N) (to the base e) |
|  |  |
| Q19. | The programmable timer device (8253) contains three independent \_\_\_\_\_\_\_\_\_\_ bit counters. |
| Option A: | 8 |
| Option B: | 16 |
| Option C: | 20 |
| Option D: | 32 |
|  |  |
| Q20. | Maximum size of segment in protected mode of 80386 is ……… |
| Option A: | 4 KB |
| Option B: | 64 KB |
| Option C: | 1 MB |
| Option D: | 4 GB |
|  |  |
| Q21. | In 80386, Size of a descriptor is ……. |
| Option A: | 1 byte |
| Option B: | 2 bytes |
| Option C: | 4 bytes |
| Option D: | 8 bytes |
|  |  |
| Q22. | In 80386 protected mechanism Type check decides ……. |
| Option A: | Read / write access |
| Option B: | Input / output access |
| Option C: | Size of segment |
| Option D: | Privilege level check |
|  |  |
| Q23. | How much physical memory can be interfaced with Pentium processor? |
| Option A: | 64 KB |
| Option B: | 1 MB |
| Option C: | 4 GB |
| Option D: | 64 TB |
|  |  |
| Q24. | Pentium is …. bit processor. |
| Option A: | 8 |
| Option B: | 16 |
| Option C: | 32 |
| Option D: | 64 |
|  |  |
| Q25. | Which group of instructions does not affect the flag? |
| Option A: | Arithmetic operation |
| Option B: | logic Operation |
| Option C: | Data transfer operations |
| Option D: | Branch operations |